REMARKS

Applicant has amended claims 1, 6 and 11 and added a new claim 21 to round out the coverage. No new matter has been added.

Claims 1-15 have been rejected under 35 USC 112, second paragraph, as being incomplete for omitting essential elements. This rejection is respectfully traversed.

The Examiner contends that the missing elements are "placing information (bits) within only specific bit positions within only the predetermined positions (of the processed image)". Applicant disagrees. The device of this invention places bits in specific bit positions of pixels located at predetermined positions of the processed image, as described below. As long as this feature is met, the device of this invention may also place bits for information other than the image data in unspecified bit positions at positions of the processed image that are not determined beforehand, because the claims are open-ended as the Examiner correctly points out. Furthermore, persons skilled in the art understand this aspect of the invention clearly from the claims.

However, in order to expedite prosecution, applicant has amended claims 1, 6 and 11 to recite "placing bits for describing information different from information of said first processed image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image." Accordingly, this rejection should be withdrawn.

Claims 1-15 have been rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,583,941 (Yoshida). Claims 1, 6 and 11 have been amended to specify that the processed image data is placed "only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image." For example, on page 12 of the specification, applicant discloses dividing an image into 64 units and then using the central pixel of these units

to embed information. The central pixel of these units would be an example of multiple bits of pixel data at predetermined positions of said processed image. Within these central pixels, information is placed in specific bit positions. In the embodiment disclosed on page 12 of the specification, these specific bit positions are the least significant bit positions of each of these central pixels.

Yoshida's device, however, searches for areas (pixels) for embedding image-scrambling data (step S1803). Yoshida's device does not specify predetermined positions of the processed image for embedding the data. The pixels chosen for receiving the data could be anywhere in the processed image data. Furthermore, in Yoshida's device, the bit positions within the chosen pixel for receiving the bits is not specified. Yoshida's device can use any bit position as long as such a bit position is equally occupied in the area chosen by the device.

Since Yoshida does not teach or suggest placing information only in specific bit positions of the pixels located only at predetermined positions of the processed image as claimed, amended claims 1, 6 and 11 should be allowed. Claims 2-5, 7-10 and 12-15, which depend from claims 1, 6 and 11, should be allowed as well.

New claim 21 recites "each of the predetermined pixels of said processed image being separated by at least one pixel from the rest of the predetermined pixels." The specification finds support, for example, on page 12, lines 8-13, and Fig. 5. As shown in Fig. 6, Yoshida discloses a group of pixels for embedding the data, which forms an array of pixels without any separation. Yoshida's device needs such an arrangement because data is embedded in a group of pixels that have a same bit level. The device of this invention avoids using such an arrangement by specifying the bit position and pixel position for embedding information other than the image data.

Attached hereto is a marked-up version of the changes made to the claims by this amendment, captioned "**Version with markings to show changes made**".

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 325772009100.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Three Times Amended) An image processing apparatus, comprising:

a processor, wherein the processor places bits for describing information different from information of image data obtained by image processing on original image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits.

6. (Three Times Amended) An image processing method comprising:

obtaining first processed image data by performing image processing on original image data; and

placing bits for describing information different from information of said first processed image data only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits.

11. (Three Times Amended) A recording medium in which a program for a computer is stored, wherein said program is one that enables the computer to perform the following processing:

placing bits for describing information different from information of image data, [said processed image data being] which is obtained by image processing on original image data, only in specific bit positions of multiple bits of pixel data only at predetermined positions of said processed image, each of the pixel data being expressed by using multiple bits.